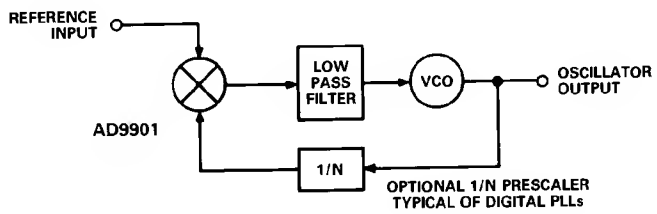
Ultrahigh Speed Phase/Frequency Discriminator

AD9901

FEATURES
Phase and Frequency Detection
ECL/TTL/CMOS Compatible
Linear Transfer Function
No "Dead Zone"
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Low Phase Noise Reference Loops
Fast-Tuning "Agile" IF Loops
Secure "Hopping" Communications
Coherent Radar Transmitter/Receiver Chains

PHASE-LOCKED LOOP



GENERAL DESCRIPTION

The AD9901 is a digital phase/frequency discriminator capable of directly comparing phase/frequency inputs up to 200 MHz. Processing in a high speed trench-oxide isolated process, combined with an innovative design, gives the AD9901 a linear detection range, free of indeterminate phase detection zones common to other digital designs.

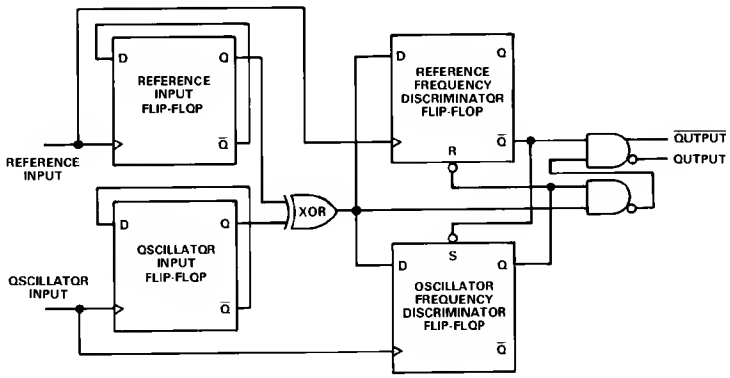
With a single +5 V supply, the AD9901 can be configured to operate with TTL or CMOS logic levels; it can also operate with ECL inputs when operated with a –5.2 V supply. The open-collector outputs allow the output swing to be matched to post-filtering input requirements. A simple current setting resistor controls the output stage current range, permitting a reduction in power when operated at lower frequencies.

A major feature of the AD9901 is its ability to compare phase/frequency inputs at standard IF frequencies without prescalers. Excessive phase uncertainty which is common with standard PLL configurations is also eliminated. The AD9901 provides the locking speed of traditional phase/frequency discriminators, with the phase stability of analog mixers.

The AD9901 is available as a commercial temperature range device, 0°C to +70°C, and as a military temperature device, –55°C to +125°C. The commercial versions are packaged in a 14-pin ceramic DIP and a 20-pin PLCC.

The AD9901 Phase/Frequency Discriminator is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9901/883B data sheet for specifications.

FUNCTIONAL BLOCK DIAGRAM



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AD9901–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage (+V_S for TTL Operation) . . . . . +7 V
Negative Supply Voltage (–V_S for ECL Operation) . . . . . –7 V
Input Voltage Range (TTL Operation) . . . . . 0 V to +5.5 V
Differential Input Voltage (ECL Operation) . . . . . 4.0 V
I_{SET} Current . . . . . 12 mA
Output Current . . . . . 30 mA
Operating Temperature Range
AD9901KQ/KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature[2]
Plastic . . . . . +150°C
Ceramic . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = +5.0 V [for TTL] or –5.2 V [for ECL], unless otherwise noted)

	Temp	Test Level	Commercial Temperature 0°C to +70°C AD9901KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
TTL Input Logic "1" Voltage	Full	VI	2.0			V
TTL Input Logic "0" Voltage	Full	VI			0.8	V
TTL Input Logic "1" Current[3]	Full	VI			0.6	mA
TTL Input Logic "0" Current[3]	Full	VI			1.6	mA
ECL Differential Switching Volt.	Full	VI	300			mV
ECL Input Current	Full	VI			20	μA
OUTPUT CHARACTERISTICS						
Peak-to-Peak Output Voltage Swing[4]	Full	VI	1.6	1.8	2.0	V
TTL Output Compliance Range	Full	V		3–7		V
ECL Output Compliance Range	Full	V		±2		V
I_{OUT} Range	Full	V		0.9–11		mA
Internal Reference Voltage	Full	VI	0.42	0.47	0.52	V
AC CHARACTERISTICS						
Linear Phase Detection Range[4]						
40 kHz	+25°C	V		360		Degrees
30 MHz	+25°C	V		320		Degrees
70 MHz	+25°C	V		270		Degrees
Functionality @ 70 MHz	+25°C	I		Pass/Fail		
POWER SUPPLY CHARACTERISTICS						
TTL Supply Current (+5.0 V)[5, 6]	+25°C	I		43.5	54.0	mA
	Full	I		43.5	54.0	mA
ECL Supply Current (–5.2 V)[5, 6]	+25°C	I		42.5	52.5	mA
	Full	I		42.5	52.5	mA
Nominal Power Dissipation	+25°C	V		218		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the service ability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Maximum junction temperature should not exceed +175°C for ceramic packages, +150°C for plastic packages. Junction temperature can be calculated by:

$t_J = PD\ (\theta_{JA}) + t_A = PD\ (\theta_{JC}) + t_C$

where:

PD = power dissipation
θ_{JA} = thermal impedance from junction to air (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)

typical thermal impedances:

AD9901 Ceramic DIP = θ_{JA} = 74°C/W; θ_{JC} = 21°C/W
AD9901 LCC = θ_{JA} = 80°C/W; θ_{JC} = 19°C/W
AD9901 PLCC = θ_{JA} = 88.2°C/W; θ_{JC} = 45.2°C/W

[3]V_L = +0.4 V; V_H = +2.4 V.

[4]R_{SET} = 47.5 Ω; R_L = 182 Ω.

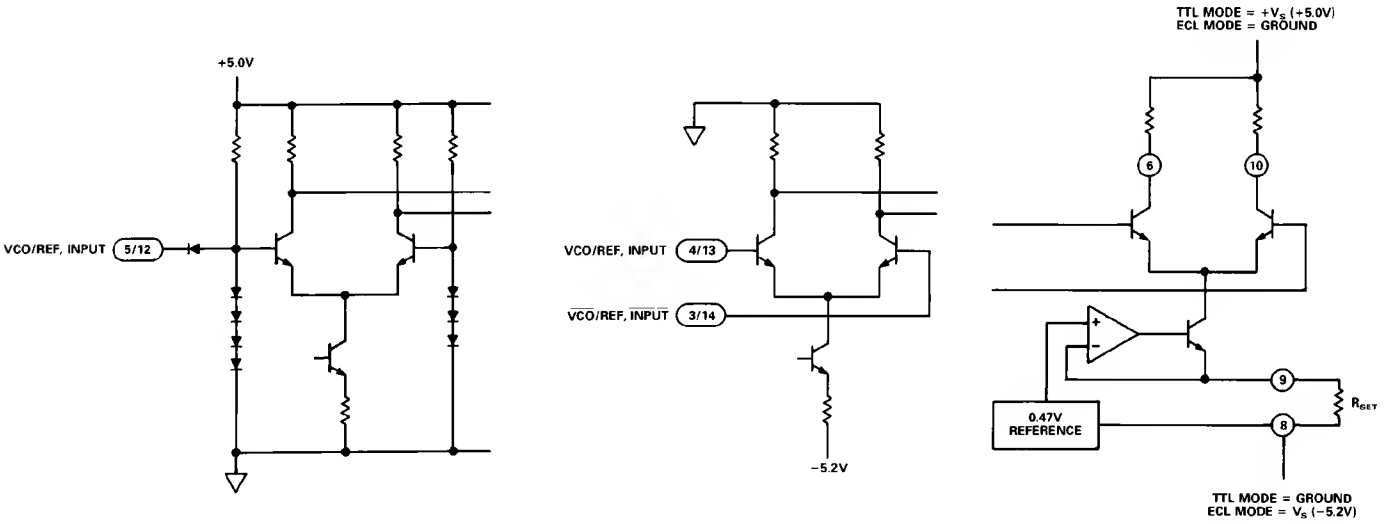
[5]Includes load current of 10 mA (load resistors = 182 Ω).

[6]Supply should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

INPUT/OUTPUT EQUIVALENT CIRCUITS

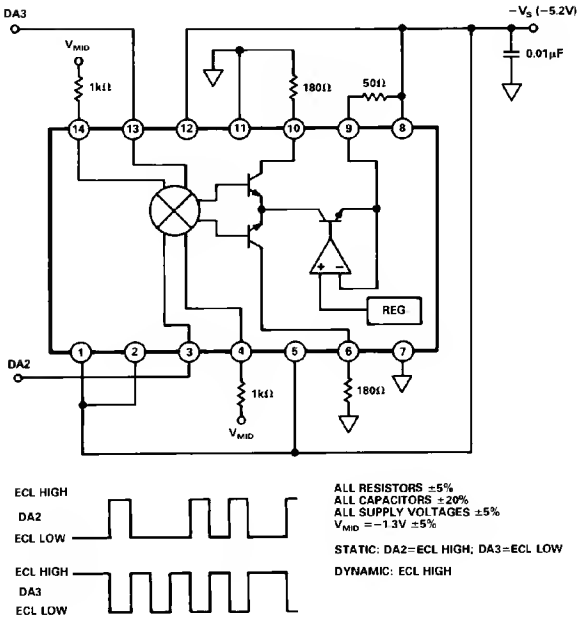
(Based on DIP Pinouts)



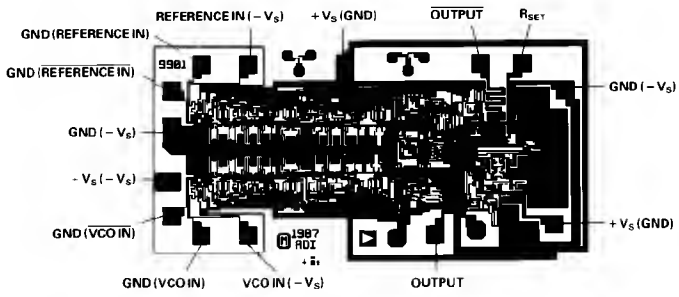
TTL Input *ECL Input* *Output*

AD9901 BURN-IN CIRCUIT

(Based on DIP ECL Pinouts)



DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	63 × 118 × 16 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	–Vs
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding

ORDERING GUIDE

Model	Temperature	Descriptions	Package Option[1]
AD9901KQ	0°C to +70°C	14-Pin Ceramic DIP	Q-14
AD9901KP	0°C to +70°C	20-Pin PLCC	P-20A
AD9901TQ/883[2]	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD9901TE/883[2]	–55°C to +125°C	20-Contact Ceramic LCC	E-20A

NOTES

[1]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip.

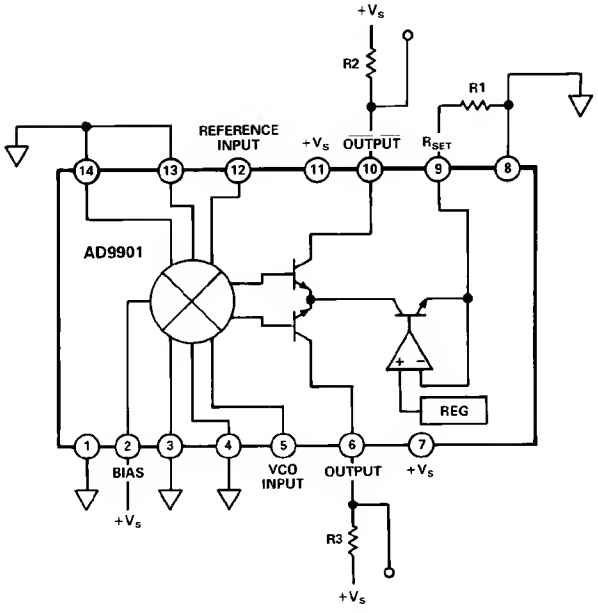
[2]For specifications, refer to Analog Devices Military Products Databook.

TTL/CMOS MODE FUNCTIONAL PIN DESCRIPTIONS

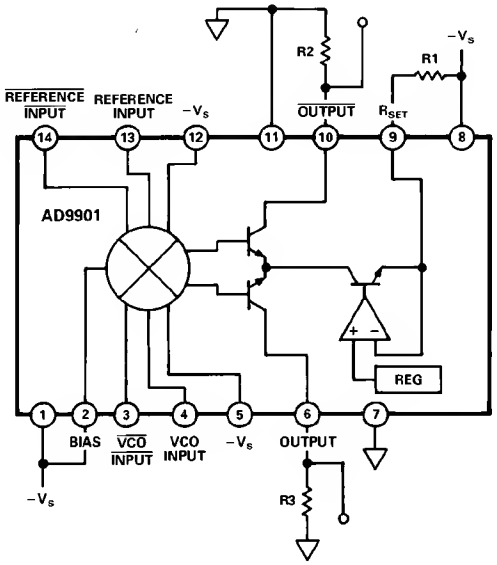
GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
$+V_S$	Positive supply connection; nominally +5.0 V for TTL operation.
BIAS	Connect to $+V_S$ (+5 V) for TTL operation.
VCO INPUT	TTL compatible input; normally connected to the VCO output signal. VCO INPUT and REFERENCE INPUT are equivalent to one another.
$\overline{\text{OUTPUT}}$	The noninverted output. In TTL/CMOS mode, the output swing is approximately +3.2 V to +5 V.
R_{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maximum full-scale output current. R_{SET} should be connected to ground through an external resistor in TTL mode. I_{SET} = 0.47 V/R_{SET} = I_{LOAD} (max.)
OUTPUT	The inverted output. In TTL/CMOS mode, the output swing is approximately +3.2 V to +5 V.
REFERENCE INPUT	TTL compatible input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent.

ECL MODE FUNCTIONAL PIN DESCRIPTIONS

$-V_S$	Negative supply connection, nominally –5.2 V for ECL operation.
BIAS	Connect to –5.2 V for ECL operation.
$\overline{\text{VCO INPUT}}$	Inverted side of ECL compatible differential input, normally connected to the VCO output signal.
VCO INPUT	Noninverted side of ECL-compatible differential input, normally connected to the VCO output signal.
OUTPUT	The noninverted output. In ECL mode, the output swing is approximately 0 V to –1.8 V.
GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
R_{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maximum full-scale output current. R_{SET} should be connected to $-V_S$ through an external resistor in ECL mode. I_{SET} = 0.47 V/R_{SET} = I_{LOAD} (max).
$\overline{\text{OUTPUT}}$	The inverted output. In ECL mode, the output swing is approximately 0 V to –1.8 V.
REFERENCE INPUT	Noninverted side of ECL-compatible differential input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent to one another.
$\overline{\text{REFERENCE INPUT}}$	Inverted side of ECL-compatible differential input, normally connected to the reference input signal. The $\overline{\text{VCO INPUT}}$ and the $\overline{\text{REFERENCE INPUT}}$ are equivalent.



TTL Mode
(Based on DIP Pinouts)



ECL Mode
(Based on DIP Pinouts)

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

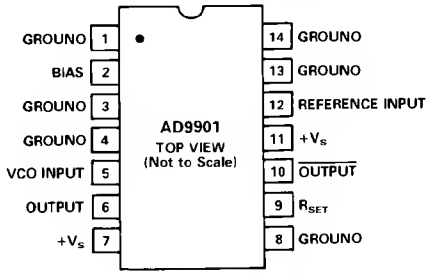
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

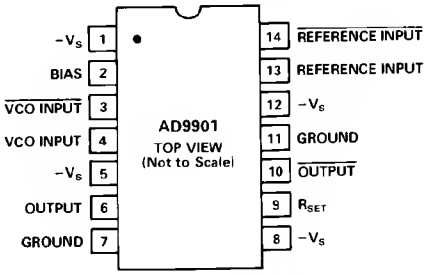
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN CONFIGURATIONS

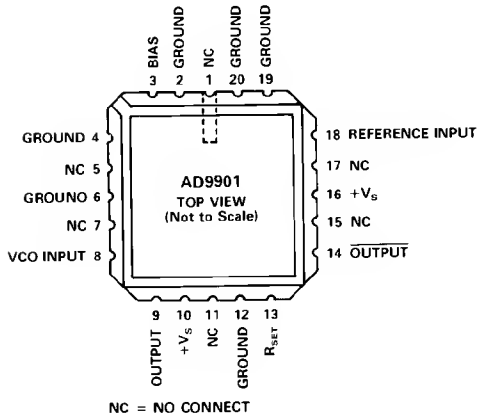
TTL DIP Pinouts



ECL DIP Pinouts

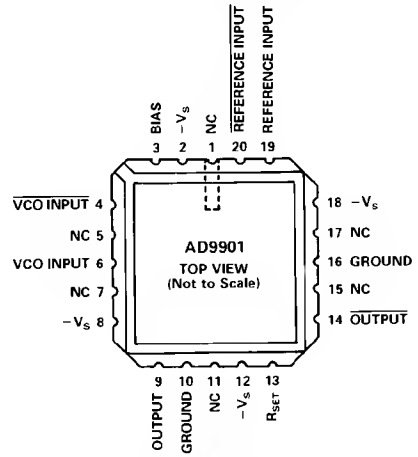


TTL LCC Pinouts



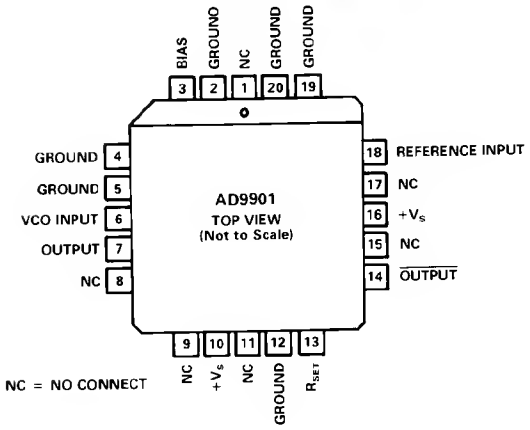
NC = NO CONNECT

ECL LCC Pinouts



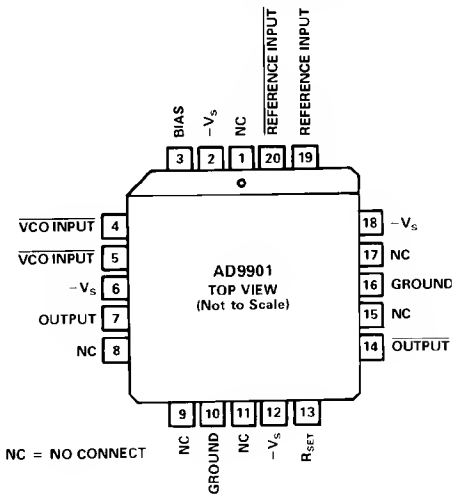
NC = NO CONNECT

TTL PLCC Pinouts



NC = NO CONNECT

ECL PLCC Pinouts



NC = NO CONNECT

THEORY OF OPERATION

A phase detector is one of three basic components of a phase-locked loop (PLL); the other two are a filter and a tunable oscillator. A basic PLL control system is shown in Figure 1.

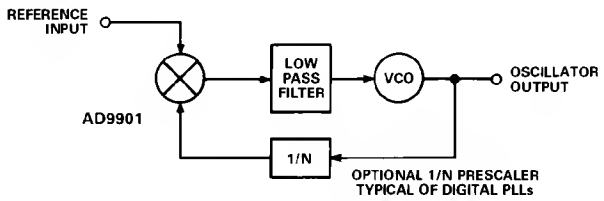


Figure 1. Phase-Locked Loop Control System

The function of the phase detector is to generate an error signal which is used to retune the oscillator frequency whenever its output deviates from a reference input signal. The two most common methods of implementing phase detectors are (1) an analog mixer and (2) a family of sequential logic circuits known as digital phase detectors.

The AD9901 is a digital phase detector. As illustrated in the block diagram of the unit, straightforward sequential logic design is used. The main components include four "D" flip-flops, an exclusive-OR gate (XOR) and some combinational output logic. The circuit operates in two distinct modes: as a linear phase detector and as a frequency discriminator.

When the reference and oscillator are very close in frequency, only the phase detection circuit is active. If the two inputs are substantially different in frequency, the frequency discrimination circuit overrides the phase detector portion to drive the oscillator frequency toward the reference frequency and put it within range of the phase detector.

Input signals to the AD9901 are pulse trains, and its output duty cycle is proportional to the phase difference of the oscillator and reference inputs. Figures 2, 3 and 4 illustrate, respectively, the input/output relationships at lock; with the

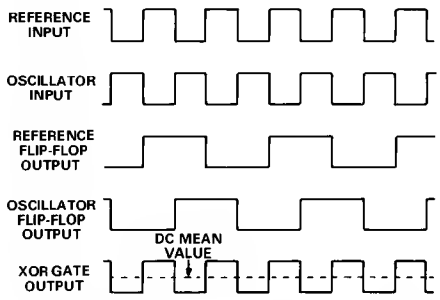


Figure 2. AD9901 Timing Waveforms at "Lock"

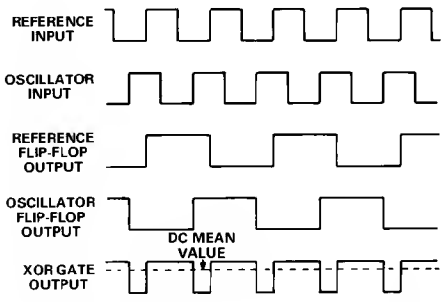


Figure 3. Timing Waveforms (ϕ_{OUT} Leads ϕ_{IN})

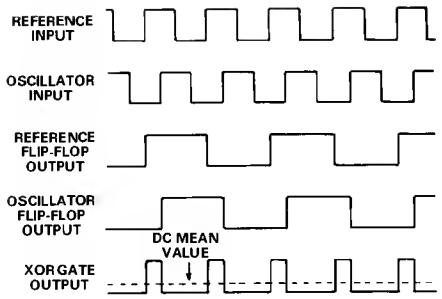


Figure 4. Timing Waveforms (ϕ_{OUT} Lags ϕ_{IN})

oscillator leading the reference frequency; and with the oscillator lagging. This output pulse train is low-pass filtered to extract the dc mean value [K_ϕ (ϕ_I – ϕ_O)] where K_ϕ is a proportionality constant (phase gain).

At or near lock (Figures 2, 3 and 4), only the two input flip-flops and the exclusive-OR gate (the phase detection circuit) are active. The input flip-flops divide both the reference and oscillator frequencies by a factor of two. This insures that inputs to the exclusive-OR are square waves, regardless of the input duty cycles of the frequencies being compared. This division-by-two also moves the nonlinear detection range to the ends of the range rather than near lock, which is the case with conventional digital phase detectors.

Figure 5 illustrates the constant gain near lock.

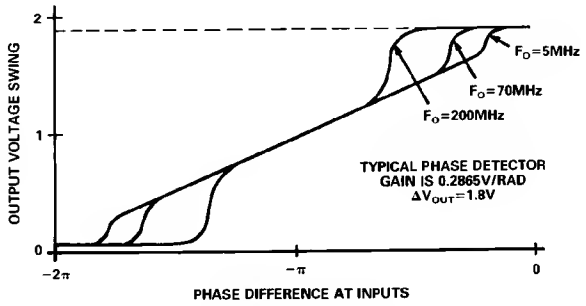


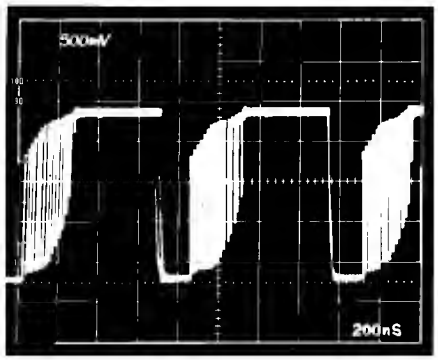
Figure 5. Phase Gain Plot

When the two square waves are combined by the XOR, the output has a 50% duty cycle if the reference and oscillator inputs are exactly 180° out of phase; under these conditions, the AD9901 is operating in a locked mode. Any shift in the phase relationship between these input signals causes a change in the output duty cycle. Near lock, the frequency discriminator flip-flops provide constant HIGH levels to gate the XOR output to the final output.

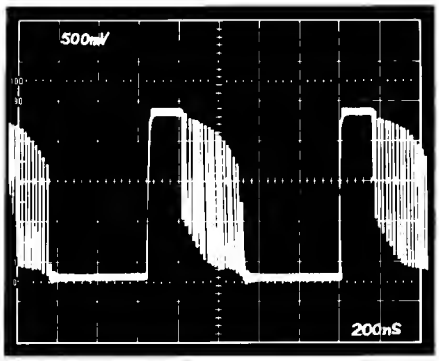
The duty cycle of the AD9901 is a direct measure of the phase difference between the two input signals when the unit is near lock. The transfer function can be stated as [$K_\phi(\phi_I - \phi_O)$](V/RAD), where K_ϕ is the allowable output voltage range of the AD9901 divided by 2 π.

For a typical output swing of 1.8 V, the transfer function can be stated as (1.8 V/2 p = 0.285 V/RAD). Figure 5 shows the relationship of the dc mean value of the AD9901 output as a function of the phase difference of the two inputs.

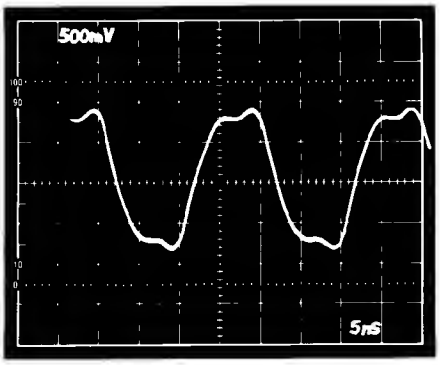
It is important to note that the slope of the transfer function is constant near its midpoint. Many digital phase comparators have an area near the lock point where their gain goes to zero,



Photograph 1. AD9901 Output Waveform($F_O \ll F_1$)



Photograph 2. AD9901 Output Waveform ($F_O \gg F_1$)



Photograph 3. AD9901 Output Waveform ($F_O = F_I = 50$ MHz)

resulting in a "dead zone." This causes increased phase noise (jitter) at the lock point.

The AD9901 avoids this dead zone by shifting it to the endpoints of the transfer curve, as indicated in Figure 5. The increased gain at either end increases the effective error signal to pull the oscillator back into the linear region. This does not affect phase noise, which is far more dependent upon lock region characteristics.

It should be noted, however, that as frequency increases, the linear range is decreased. At the ends of the detection range, the reference and oscillator inputs approach phase alignment. At this point, slew rate limiting in the detector effectively increases phase gain. This decreases the linear detection by nominally 3.6 ns. Therefore, the typical detection range can be found by calculating $[(1/F - 3.6\text{ ns})/(1/F)] \times 360°$. As an example, at 200 MHz the linear phase detection range is ±50°.

Away from lock, the AD9901 becomes a frequency discriminator. Any time either the reference or oscillator input occurs twice before the other, the Frequency High or Frequency Low flip-flop is clocked to logic LOW. This overrides the XOR output and holds the output at the appropriate level to pull the oscillator toward the reference frequency. Once the frequencies are within the linear range, the phase detector circuit takes over again. Combining the frequency discriminator with the phase detector eliminates locking to a harmonic of the reference.

Photograph 1 shows the effect of the "Frequency Low" flip-flop when the oscillator frequency is much lower than the reference input. The narrow pulses, which result from cycles when two positive reference-input transitions occur before a positive VCO edge, increase the dc mean value. Photograph 2 illustrates the inverse effect when the "Frequency High" flip-flop reacts to a much higher VCO frequency.

Photograph 3 shows the output waveform at lock for 50 MHz operation. This output results when the phase difference between reference and oscillator is approximately –πRad.

AD9901 APPLICATIONS

The figure below illustrates a phase-locked loop (PLL) system utilizing the AD9901. The first step in designing this type of circuit is to characterize the VCO's output frequency as a function of tuning voltage. The transfer function of the oscillator in the diagram is shown in Figure 6.

Next, the range of frequencies over which the VCO is to operate is examined to assure that it lies on a linear portion of the

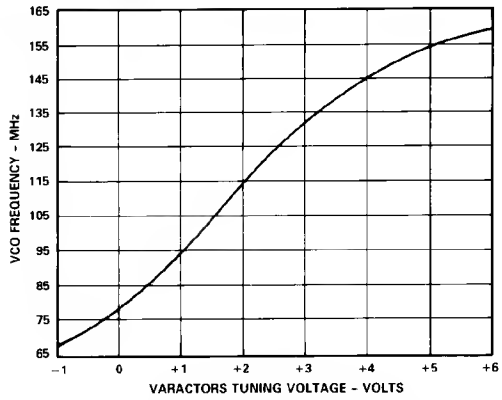


Figure 6. VCO Frequency vs. Voltage

transfer curve. In this case, frequencies from 100 MHz to 120 MHz result from tuning voltages of approximately +1.5 V to +2.5 V. Because the nominal output swing of the AD9901 is 0 V to –1.8 V, an inverting amplifier with a gain of 2 follows the loop filter.

As shown in the illustration, a simple passive RC low-pass filter made up of two resistors and a tantalum capacitor eliminates the need for an expensive high speed op amp active-filter design. In this passive-filter second-order-loop system, where n=2, the damping factor is equal to:

$$\delta = 0.5\,[K_O K_d / n(\tau_1 + \tau_2)]^{1/2}\,[\tau_2 + (n/K_O K_d)]$$

and the values for T1 and T2 are the low-pass filter's time constants R1C and R2C. The gain of 2 of the inverting stage, when combined with the phase detector's gain, gives:

$$K_d = 0.572\text{ V/RAD}$$

With $K_O = 115.2$ MRAD/s/V, τ_1 equals 1.715s, and τ_2 equals 3.11×10^{-4}s for the required damping factor of 0.7. The illustrated values of 30 Ω (R_1), 160 Ω (R_2), and 10 µF (C) in the diagram approximate these time constants.

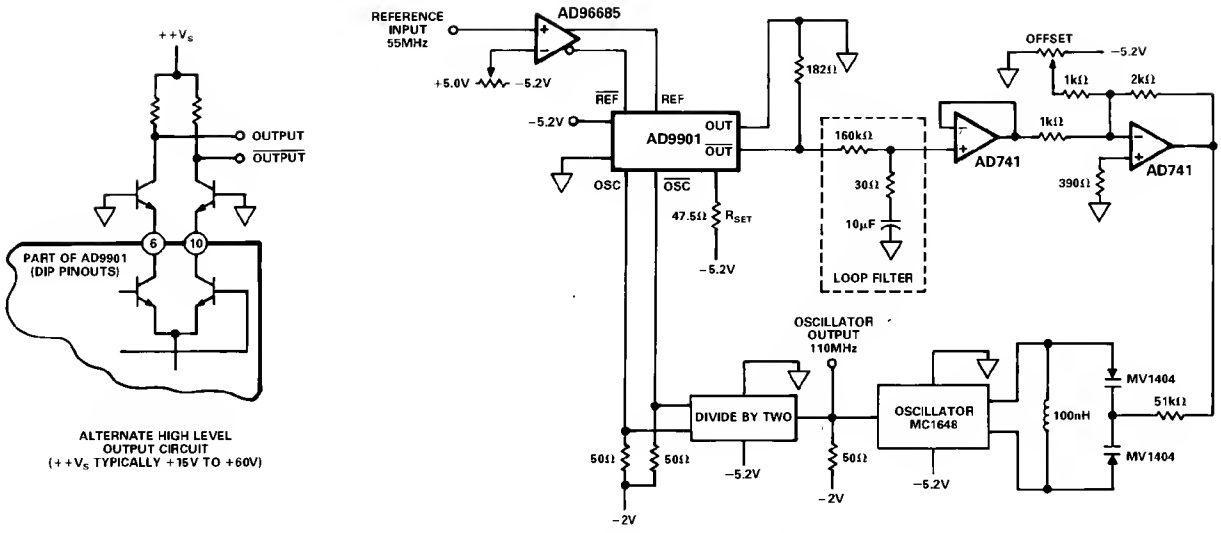
The gain of the RC filter is:

$$V_O/V_I = (1 + sR_2C)/[1 + s(R_1 + R_2)C].$$

Where $K_O K_d \gg \omega_n$, the system's natural frequency:

$$\omega_n = [K_O K_d / n(\tau_1 + \tau_2)]^{1/2} = 4.5\text{ kHz}.$$

For general information about phase-locked loop design, the user is advised to consult the following references: Gardner, Phase-Lock Techniques (Wiley); or Best, Phase Locked Loops (McGraw-Hill).

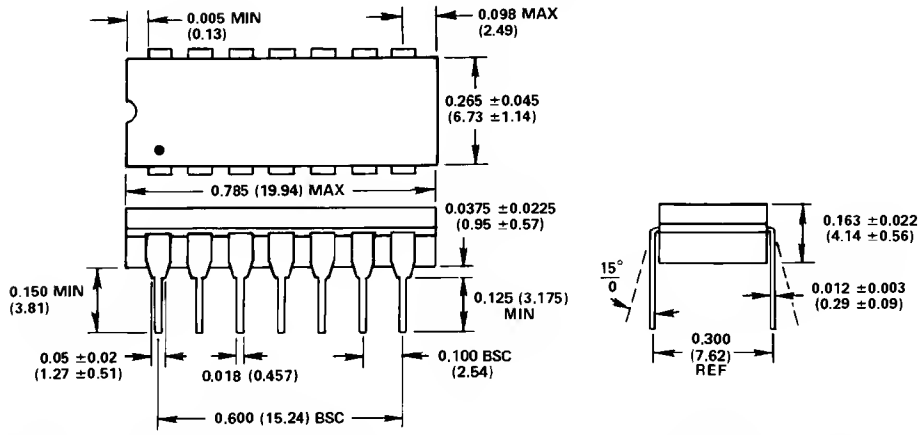


Phased-Locked Loop Using AD9901

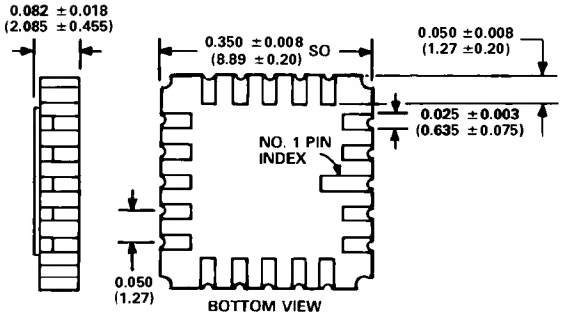
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Cerdip (Q) Package



Leadless Ceramic Chip Carrier (E) Package



Plastic Leaded Chip Carrier (P) Package